CLAIMS

What is claimed is:

1. An integrated transceiver circuit, comprising:

a digital transmitter path that provides a signal from a digital input, the transmitter path including at least one digital predistorter that predistorts the digital input to mitigate nonlinearities associated with a power amplifier;

a receiver path associated with the digital transmitter path;

a coupling element that provides the signal from the transmitter path to the receiver path; and

a signal evaluator that determines values for at least one parameter associated with the digital predistorter based on the signal.

2. The circuit of claim 1, the transmitter path comprising a gain normalization component that transfers the digital input from a normalized domain to a domain that is dependent on process, voltage, and temperature (PVT) variations.

3. The circuit of claim 2, the digital predistorter preceding the gain normalization component on the transmitter path, such that the digital predistorter predistorts the digital input in the normalized domain.

4. The circuit of claim 1, the power amplifier comprising an internal power amplifier that is integrated into the integrated transceiver circuit.

5. The circuit of claim 4, the internal power amplifier comprising a Class E switching amplifier.

6. The circuit of claim 4, the digital transmitter path comprising an amplitude modulated path that provides a supply to the internal power amplifier

from a first digital input, and a phase modulated path that provides a radio frequency input to the internal power amplifier from a second digital input.

7. The circuit of claim 6, the phase modulated path comprising a digitally controlled oscillator.

8. The circuit of claim 7, the phase modulated path comprising a gain normalization component that adjusts the second digital input for PVT variations associated with the digitally controlled oscillator.

9. The circuit of claim 6, the phase modulated path comprising a digital predistorter that adjusts the second digital input to mitigate nonlinearities associated with the power amplifier.

10. The circuit of claim 6, the amplitude modulated path comprising a digital predistorter that adjusts the first digital input to mitigate nonlinearities associated with the power amplifier.

11. The circuit of claim 6, the amplitude modulated path comprising a gain normalization component that adjusts the first digital input for PVT variations associated with the internal power amplifier.

12. The circuit of claim 1, the power amplifier comprising an external power amplifier that is external to the integrated transceiver circuit.

13. The circuit of claim 12, the power amplifier further comprising an internal power amplifier, the output of the internal power amplifier being provided to the external power amplifier.

14. The circuit of claim 12, the digital transmitter path comprising an amplitude modulated path that controls the supply to the external amplifier

according to a first digital input, and a phase modulated path that provides a radio frequency input to the external power amplifier according to a second digital input.

15. The circuit of claim 14, the phase modulated path comprising a digitally controlled oscillator.

16. The circuit of claim 15, the phase modulated path comprising a gain normalization component that adjusts the second digital input for PVT variations associated with the digitally controlled oscillator.

17. The circuit of claim 14, the phase modulated path comprising a digital predistorter that adjusts the second digital input to mitigate nonlinearities associated with the power amplifier.

18. The circuit of claim 14, the amplitude modulated path comprising a digital predistorter that adjusts the first digital input to mitigate nonlinearities associated with the power amplifier.

19. The circuit of claim 14, the amplitude modulated path comprising a gain normalization component that adjusts the first digital input for PVT variations associated with the digitally controlled oscillator.

20. The circuit of claim 1, the transmitter path being operative to alternate between a saturation mode, in which the power amplifier is driven at saturation, and a linear mode, in which the power amplifier operates within a linear range.

21. A method of calibrating a predistortion component in a transceiver system, comprising:

providing a first digital signal, containing amplitude information related to a desired analog signal, to a transmitter path;

providing a second digital signal, containing phase information related to the desired analog signal, to the transmitter path;

predistorting at least one of the first digital signal and the second digital signal in the digital domain according to at least one predistortion parameter;

generating an analog signal from the first digital signal and the second digital signal; and

processing the analog signal at a receiver path associated with the transmitter path to determine values for the at least one predistortion parameter.

22. The method of claim 21, further comprising converting the first digital signal and the second digital signal from associated normalized domains to process, voltage, and temperature (PVT) dependent domains.

23. The method of claim 21, further comprising adjusting the value of the first digital signal to switch an associated power amplifier from a linear mode of operation to a saturated mode of operation.

24. An integrated transceiver circuit, comprising:

means for producing a digital input;

means for predistorting the digital input to mitigate nonlinear error associated with a power amplifier according to one or more predistortion parameters;

means for converting the digital input from a normalized domain to a process, voltage, and temperature (PVT) dependent domain;

means for generating an analog signal from the digital input; and

means for analyzing the analog signal to determine appropriate predistortion parameters for the means for predistorting.

25. The circuit of claim 24, the means for generating the analog signal comprising means for synthesizing a radio frequency signal from a digital input.

26. The circuit of claim 24, the means for analyzing the analog signal including means for applying a direct current (DC) offset to the signal.